Development of 128M DRAM by Stacked Packaging Technology

Packaging Technology Team

Background of the Development

- *Recently, the users system environments are rapidly changed to higher performance.*
- *So, they required high memory density.*
- *But memory makers could not satisfy their requirements.*
- *Many system makers request their memory supplier high density memory solution.*
- *3D Package is one of the solutions as high density memory*
- *Stacked 128M DRAM is one of our example.*

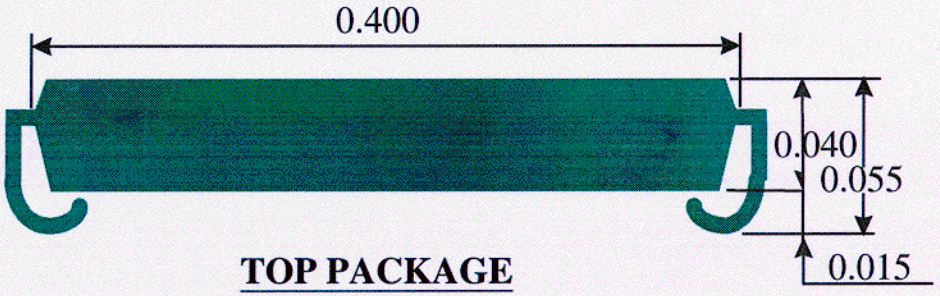
Text environments

1990's

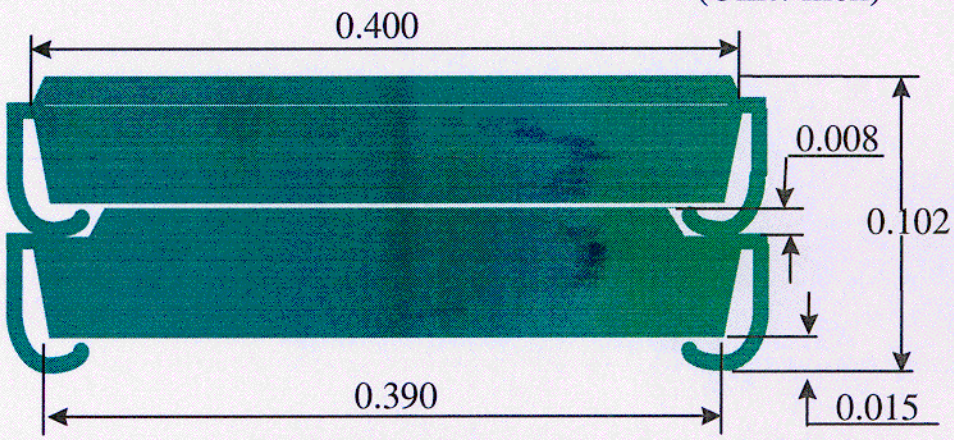
Graphical environments

What is SAMSUNG's Stacked package.

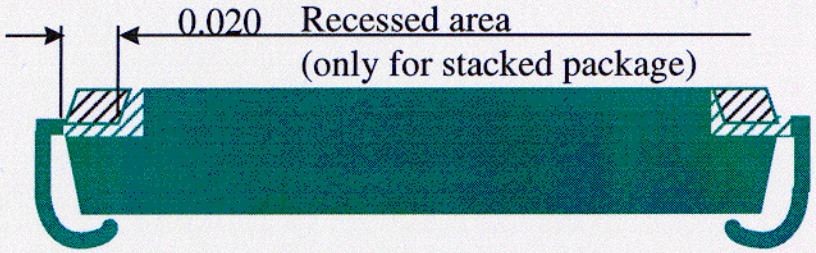
(Unit: inch)



TOP PACKAGE



STACKED PACKAGE



BOTTOM PACKAGE

TSOP	Stacked Package	SOJ
[47mil = (A)]	[102mil (2.6x2A)]	[148mil (3.8x3A)]

Thickness: A little thicker than TSOPII
Width: Same as TSOPII & SOJ
Lead: J type

Total Package thickness(compatible to SOJ)
- In case of two-stack package,
  Two-thirds thickness of SOJ

Better Solder Joint Reliability, compared to TSOPII
Reduced PCB Space by J type package

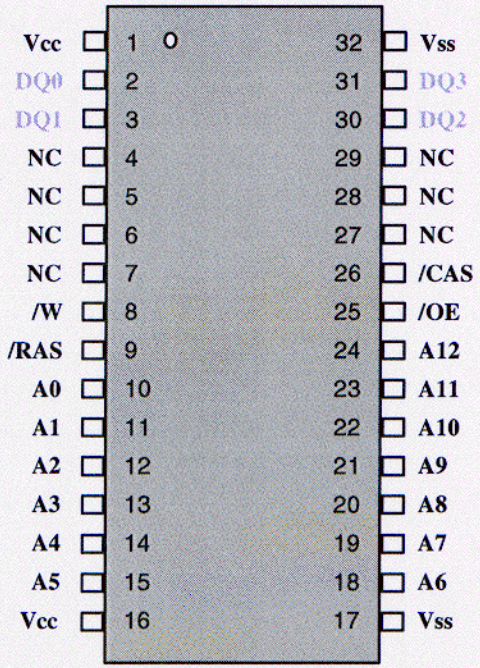
Why Stacked 128M DRAM (2 Stack) !

- **Easy Manufacturing.**
  - > Using the proven process(Conventional plastic package process)
  - > Only two stack
- **Using the same SMT foot print.**
  - > It is not needed to change the PCB design.
- **Reliable**
  - > Better reliability & performance than conventional plastic package
- **Most important thing is Cost Effective.**
  - > Dose not need new chip design and process .
  - > Dose not change current process

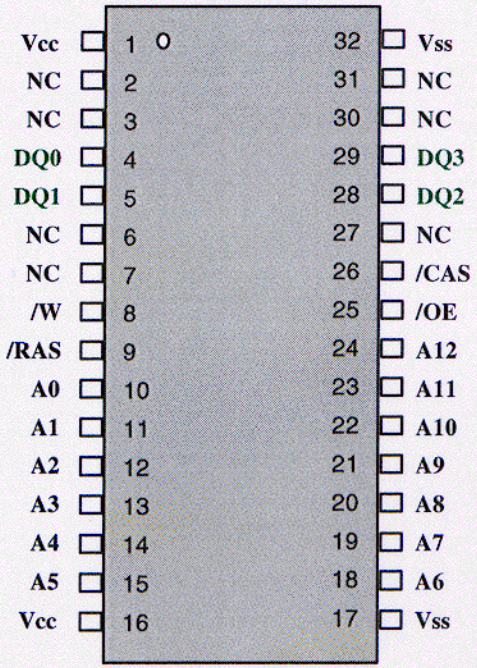
Design concept of Stacked 128M DRAM

1. Stacked 16Mx8(16Mx4*2) DRAM Pin Configuration

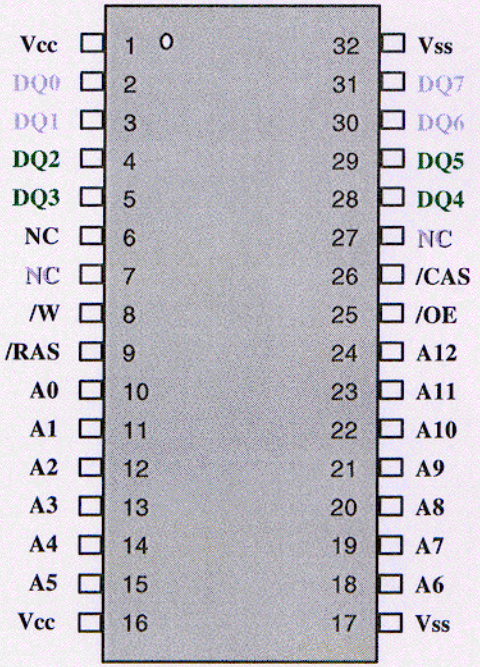
16Mx4(**Top**)
32 TSOJ



16Mx4(**Bottom**)
32 TSOJ



Stacked 16Mx8(16Mx4)
32 TSOJ



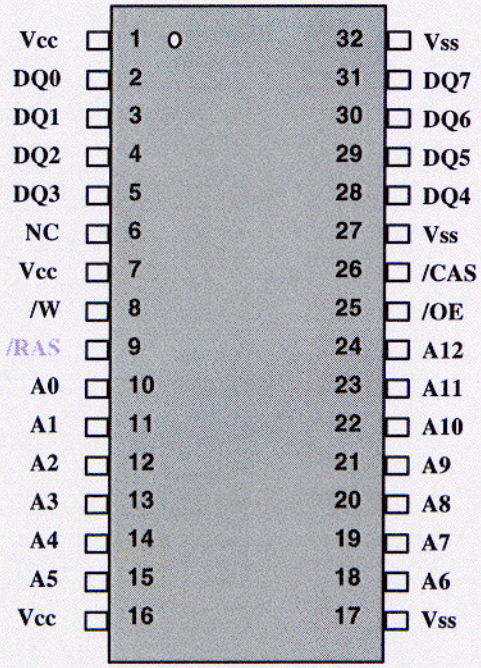
- **Top package** uses the same lead frame that of 16Mx8 DRAM.

- **Bottom package** uses the same lead frame but the wire bonding is different(**bonding option**).

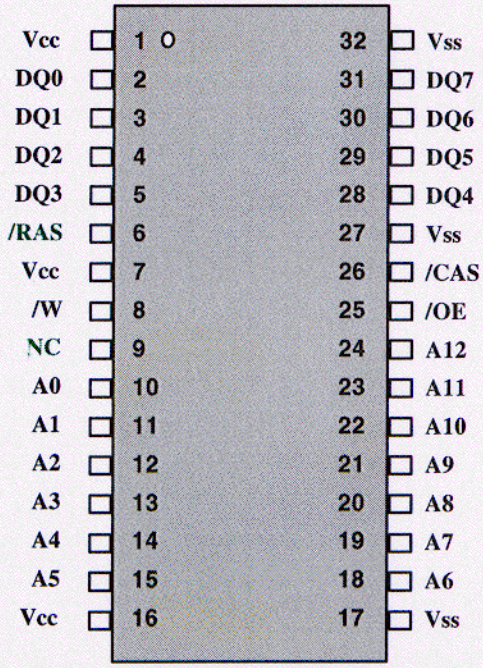
- Same pin configuration as 8Mx8 except center Vcc/Vss

2. Stacked 16Mx8(8Mx8*2) DRAM Pin Configuration

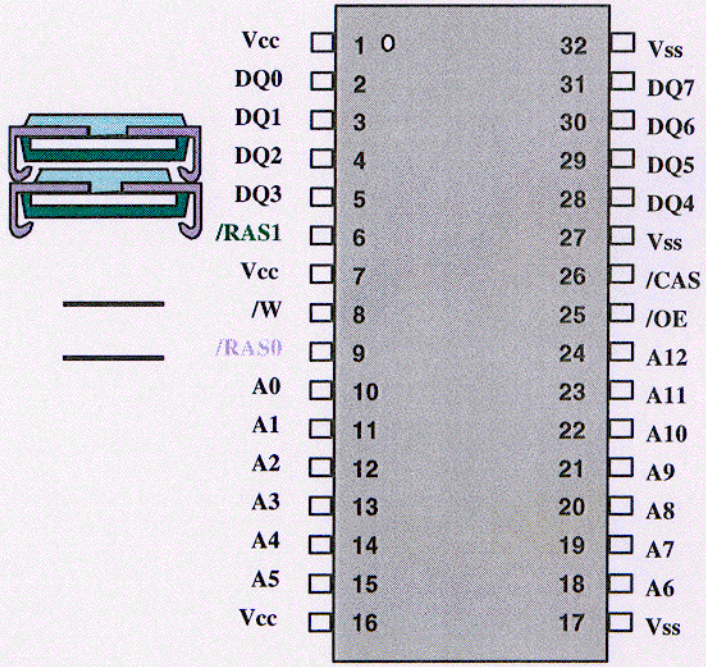
8Mx8(**Top**)
32 TSOJ



8Mx8(**Bottom**)
32 TSOJ



Stacked 16Mx8(8Mx8)
32 TSOJ



- **Top package** uses the same lead frame that of 8Mx8 DRAM.

- **Bottom package** uses the same lead frame but the wire bonding is different(**bonding option**).

- **Dual RAS Stacked 16Mx8** same pin configuration as 8Mx8 except pin 6(RAS1)

Process Review.

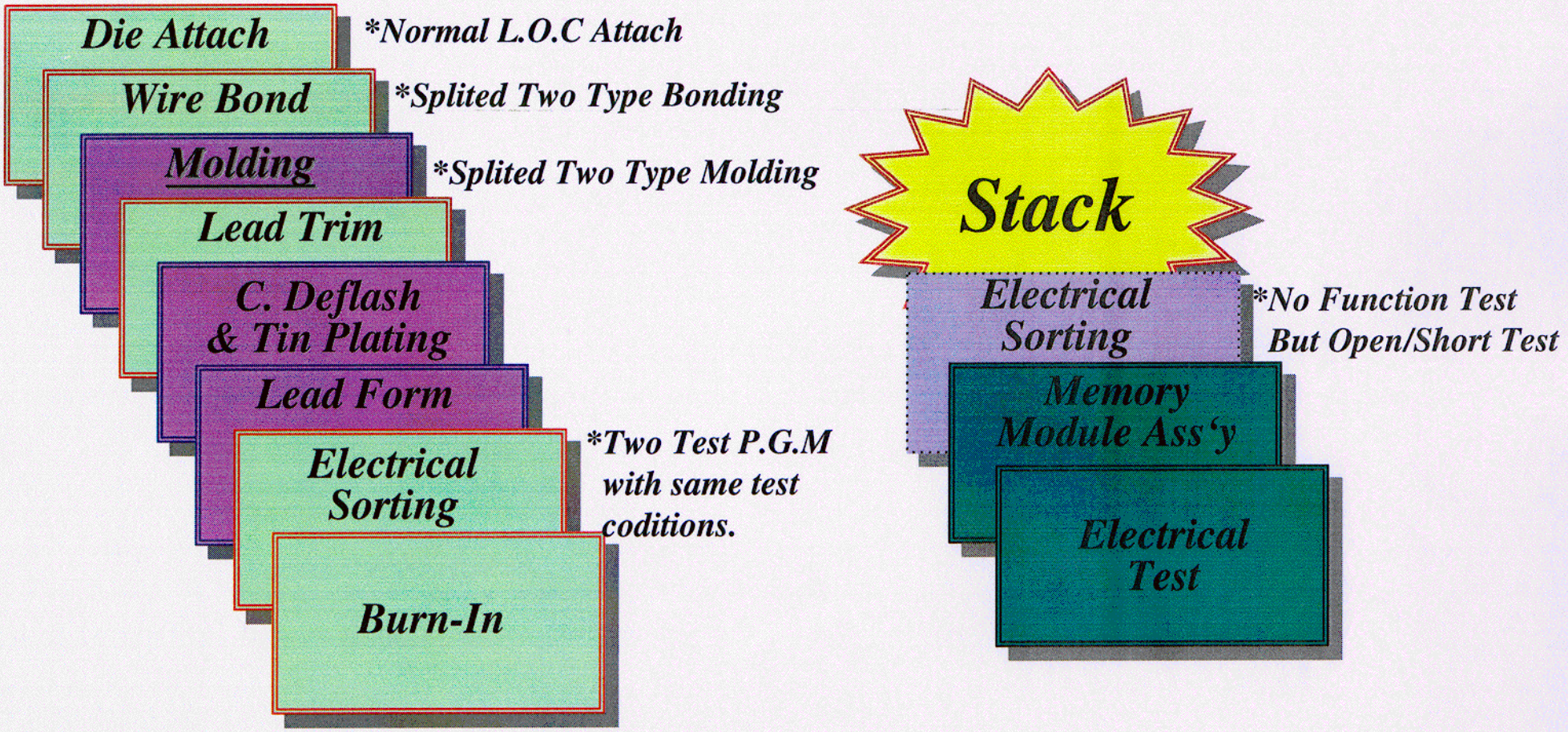
<Our Stacked packaging process is based on the Conventional process>

Issues on developing Stacked Package

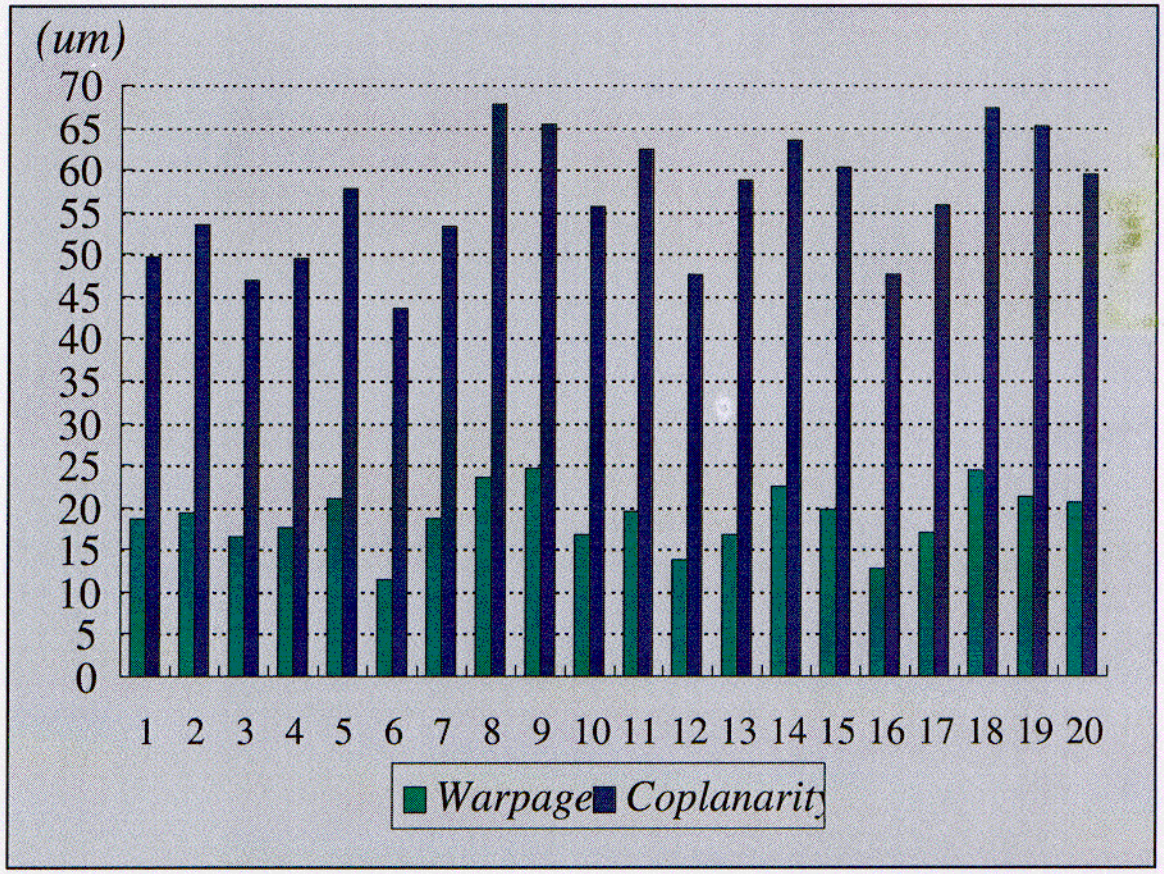
- *Warpage and Coplanarity.*
- *Molding resin bleed and In-line plating for bottom package.*
- *Lead Plating Thickness and adding Solder Paste.*
- *Stacking Process*

Process Flow

Conventional Plastic Packaging process + Stack Process

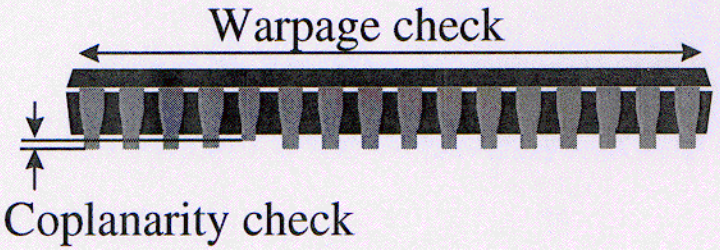


Warpage and Coplanarity



* Warpage; **below 25um**

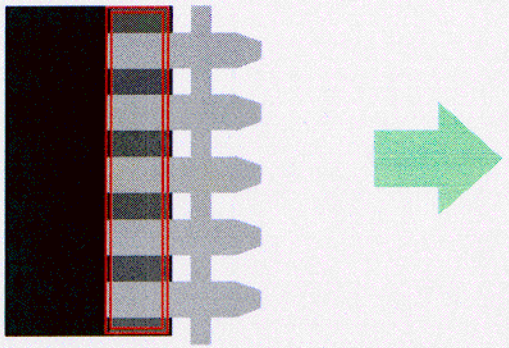
* Coplanality; **below 70um**



Resin bleed and Chemical Deflash

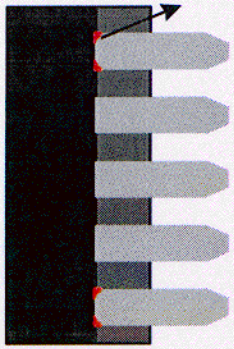
Measurement of mold resin bleed

Sample	Value(mm)	Sample	Value(mm)	Sample	Value(mm)	Sample	Value(mm)
1	0.45	6	0.47	11	0.48	16	0.53
2	0.51	7	0.49	12	0.52	17	0.52
3	0.50	8	0.51	13	0.48	18	0.54
4	0.52	9	0.48	14	0.52	19	0.48
5	0.51	10	0.52	15	0.49	20	0.51

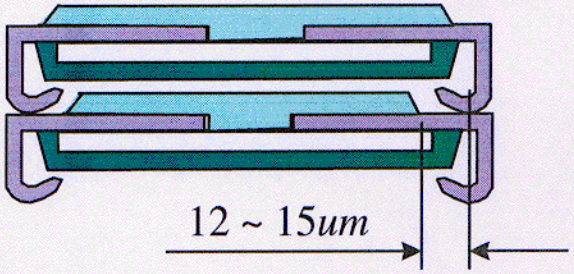


After Molding (X20)
Resin bleed appeared

Heavy Flash (5mil max.)



After Tin Plating
With Chemical Deflash (X20)



Body Edge to Joint Center
is 12 ~ 15*um*

Lead Tin Plating and Solder Paste

1. Lead Tin plating

1) Material ; Sn /Pb(85:15)

2) Process Evaluation

- Purpose : Obtain upto 20*um* Tin Plating Thickness (Using interconnection material of the stacked package with flux. -both top and bottom packages.)

(um)

Split	Condition	Result	Remark
1st (10 Strip)	- 90A - 3.0m/min	- Avg.;22.04 - Max.;24.26 - Min.;19.01	- Normal Condition
2nd (10 Strip)	- 90A - 2.5m/min	- Avg.;23.89 - Max.;26.93 - Min.;22.36	*Current = 65A
3rd (30 Strip)	- 90A - 2.0m/min	- Avg.;23.59 - Max.;26.79 - Min.;20.47	*Time = 4.2m/min
Mass (800 Strip)	- 90A - 2.5m/min	- Avg.;19.50 - Max.;21.67 - Min.;17.63	

2. Adding Solder Paste

1) Material : Sn/Pb(63:37)
Sn/Ag(96.5:3.5)*

* ; Not Reported this paper.

2) Viscosity change : 80K ,100K, 300K (CPS)

3) Printing Area :

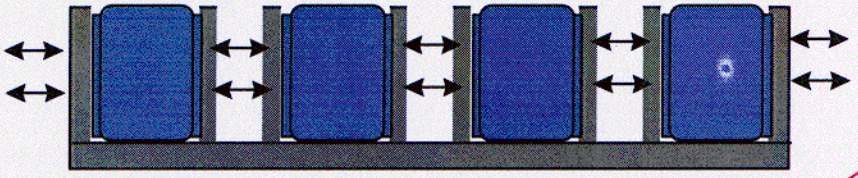
- Only the seating plane of top package (Rounded edge)

Stacking Process Flow

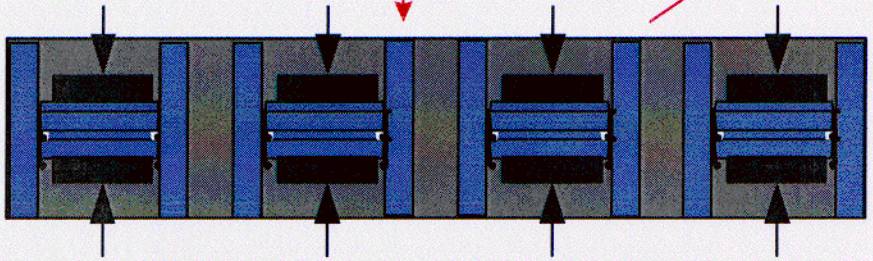
Tray(JEDEC Type)
(8x12)

Pick & Place

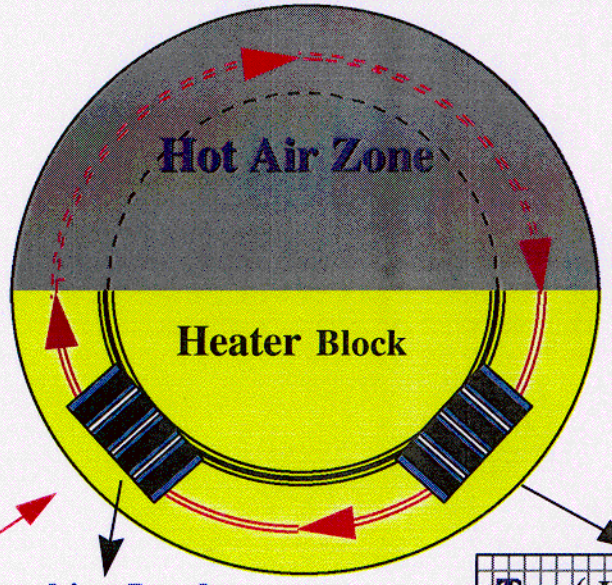
Package Pick-up
(Bottom & Top)



Stacking Jig (for right & left Alignment)



Loading in **Stacking Loader**
(for top and bottom Stack-- 1kg /cm²)



Stacking Loader

Tray(JEDEC Type)
(8x12)

Lead Coplanarity : Max. 3mil

Stacking Process(2/2); Diagram Explanation

1. Move Bottom Package from **Tray** to **Stacking Jig** , using **Pick & Place** equipment .

2. Put Top Package on the Metal Plane(containing Solder Paste) to apply Solder Paste into Top Package lead(Sitting Plane).

3. Move Top Package(containing Solder Paste) on Bottom Package which was put already in **Stacking Jig** in order for raw stacked component to make right & left(side) alignment.

4. Transfer from **Stacking Jig** to **Stacking Loader** in order for raw stacked component to make top & bottom alignment.

5. Pass **Stacking Loader**(containing raw stacked component) through round-type **Hot Air Zone**(soldering zone).

6. After Stacked component on **Stacked Loader** passing through round-type **Hot Air Zone** , solder joint layer between top and bottom package. is formed and stacked component process is finished.

7. Stacked component is transferred from **Hot Air zone** to **Tray**.

Tin Plating Thickness , Warpage & Coplanarity Evaluation

1. Evaluation Item

No.	Warpage	Plating	Coplanarity	Quarity
1	N	2.5m/min.	2mil	16
2	N	2.5m/min.	3mil	16
3	N	2.0m/min.	3mil	16
4	D	2.5m/min.	2mil	16
5	D	2.5m/min.	3mil	16

* N ; Convex Shape warpage
D ; Concave Shape warpage

2. Result

No	Number of R	Number of S	Number of F	Remark
1	23	17	472	R+S=40
2	34	8	470	R+S=42
3	6	-	506	R+S=6
4	14	19	479	R+S=33
5	31	30	451	R+S=61

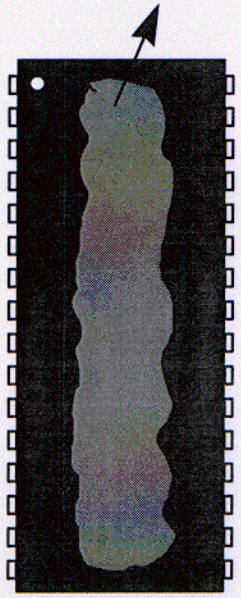
F = Full Fillet / R = Recessed Fillet / S = Side Fillet

3. Problems

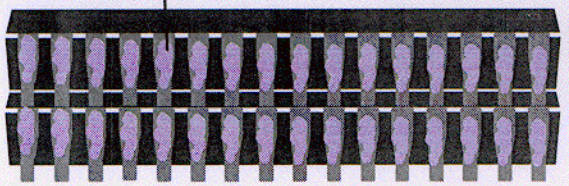
- Irregular solder joint Shape
- Package Contamination
- Package Lead discolor
- Weak Joint Strength

Due to **Flux Fume & **Small Amount of Tin***

Contamination
(Irreadable Marking)



Discolor & Contamination
(Contact Fail at E/L Test)



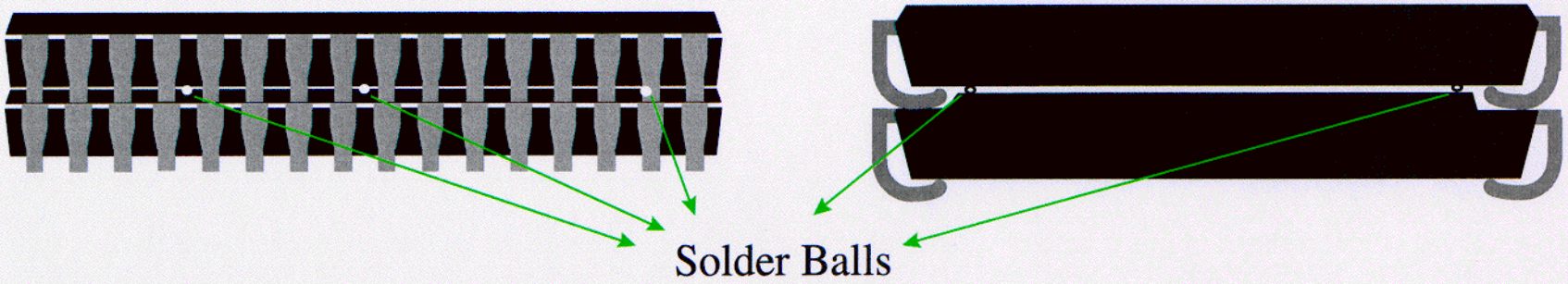
Solder Paste

- *We had been evaluate several conditions.*
  - Normal solder paste ; Sn/Pb (63:37) for normal screen printing
  - High temperature solder ; Sn/Ag(96.5:3.5)
  - Increase viscosity step by step ; 80K --> 150K --> 300K CPS
- *Final result*
  - Solder Paste viscosity ;300,000cps
  - Material ; Sn/Pb (63/37)

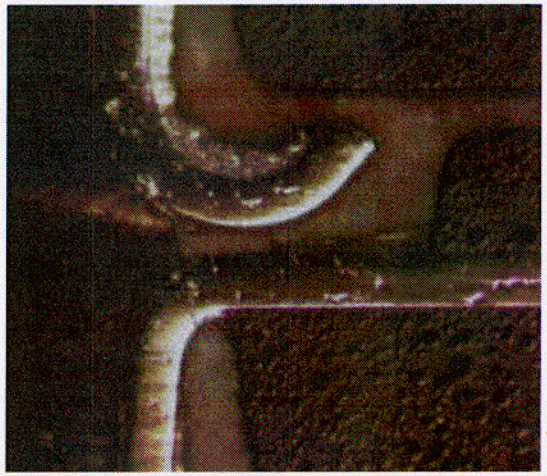
  > Sn/Ag(96.5:3.5) is more difficult process control & less mass productivity
- *Issues*

  > Solder Balls(max. 7mil) are placed between top package and bottom package, and lead and lead .(During the alignment of two packages under the Staking Jig)

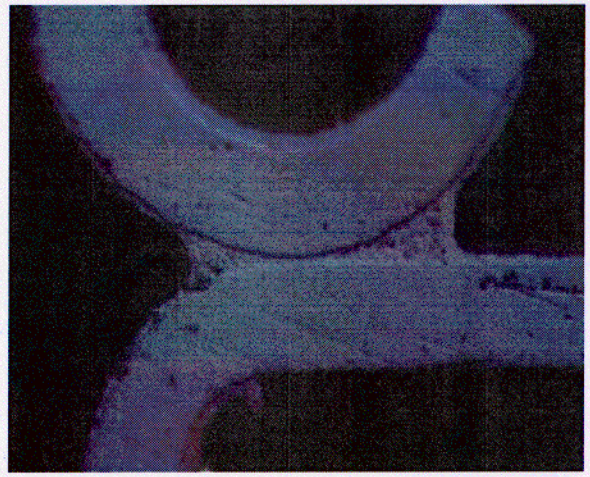
  > But they could be removed.



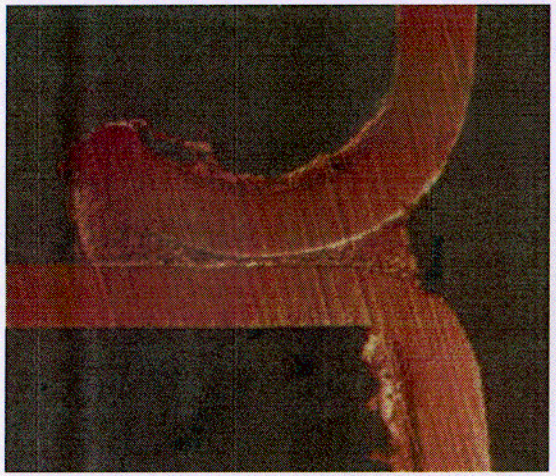
Solder Joint View 1



(Coplanairy issue)

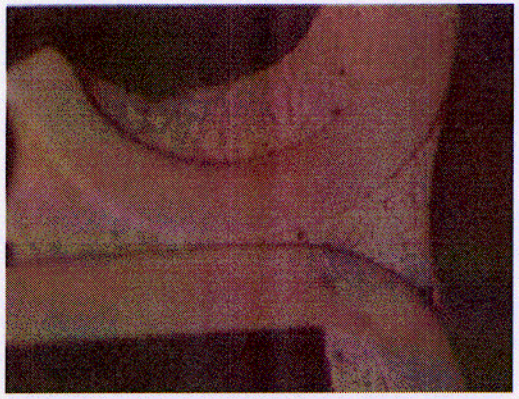


(Plating only)



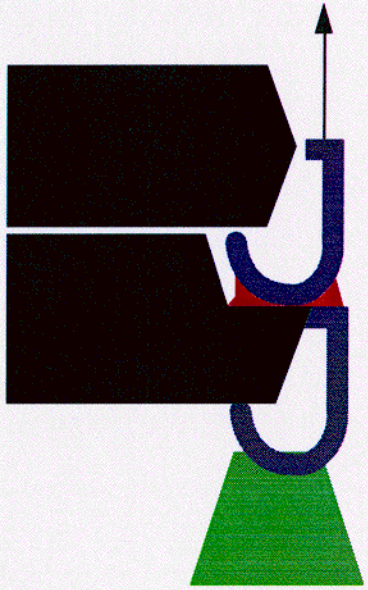
(Plating only)

(Solder Paste)



(Solder Paste)

Lead Pull Strength Test



Top Lead -- Pull

Spec. : 500g/pin (min.)

Bottom Lead

-- Fix on the stage

Result

- Tin Plating Only ; 250 ~ 1115g/Pin
- Solder Paste ; 770 ~ 1950g/Pin

Summary of electrical function test

1st test ; Unit & Stacked Package

Device		Room Temp Sort	Hot Sort (Burn-In)	Stack	Remarks
16Mx4	Top	674/690	627/672	602/612 (98.26%)	- Fail parts are almost O/S Fail (Misalign/Bent Lead/Jamming)
	Bottom	673/695	612/673		
	Yield	97.25%	92.11%		
8Mx8	Top	691/716	619/691	581/605 (96.33%)	- Rework & Retest 100% Good
	Bottom	697/716	620/697		
	Yield	96.93%	89.3%		

2nd test ; Stacked Package (For verification of stack)

Device		Room Temp Sort	Remarks
16Mx4	50ns	184/193 (95.34%)	- Fail parts are almost O/S Fail. (Excess Solder/Misalign / Jamming on hander)
	60ns	479/488 (98.35%)	

Stacked DRAM Reliability Test Data

◆ Unit Package & Stacked Module Pre-condition Data

Temp. / PKG..	85 °C/65% (168hrs)	Temp. Cycle (65 ~ 155 °C)	IR.. Reflow (235 °C)	Remark
Top Package	0/116			
Bottom Package	0/116			
Stacked Package With PCB	0/10 Modules (Visual Inspection)			-32EA Stacked Package Mount.

◆ Unit Package Long Term Reliability Data

- Soak: 85C / 65%, 1000Hrs
- Pressure Cooker Test (121 C , 2 atmosphere, 240 Hrs)
- Temperure Cycle Test (-65 C~ 155 C / 1000 cycles)

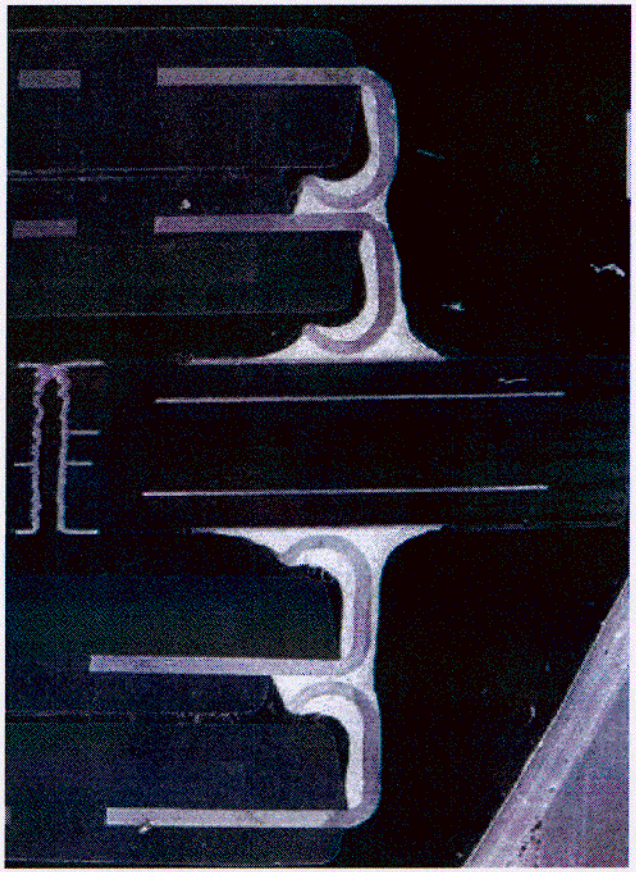
➡ ***All passed***

◆ Stacked Temperature Cycle Data

Cycle / S/J		300cyc.	600cyc.	1000cyc.	Remark
Solder Joint (0 ~ 125°C)	Dummy stack	0/116	0/116	0/116	32TSOJ Stack

Solder Joint View 2

>> Double sided reflow soldering + Procondition <<

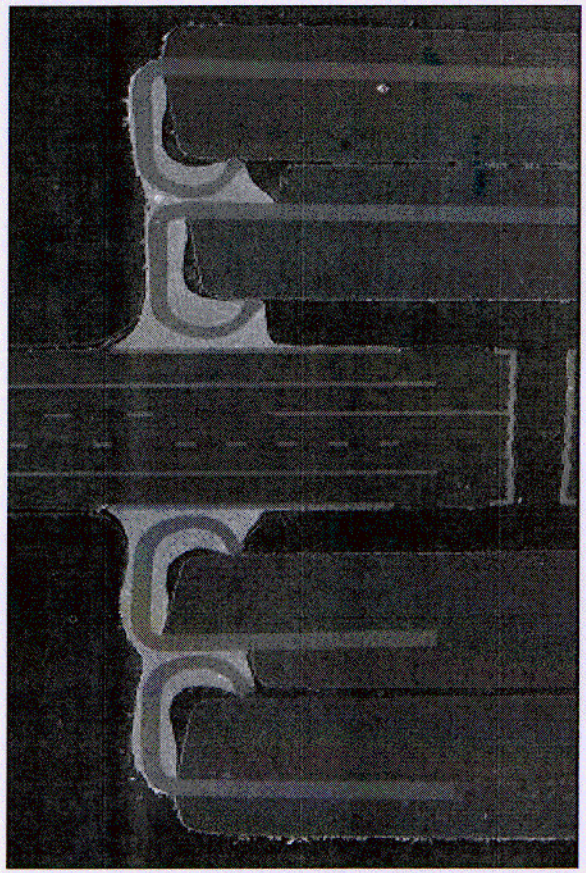


★Top side

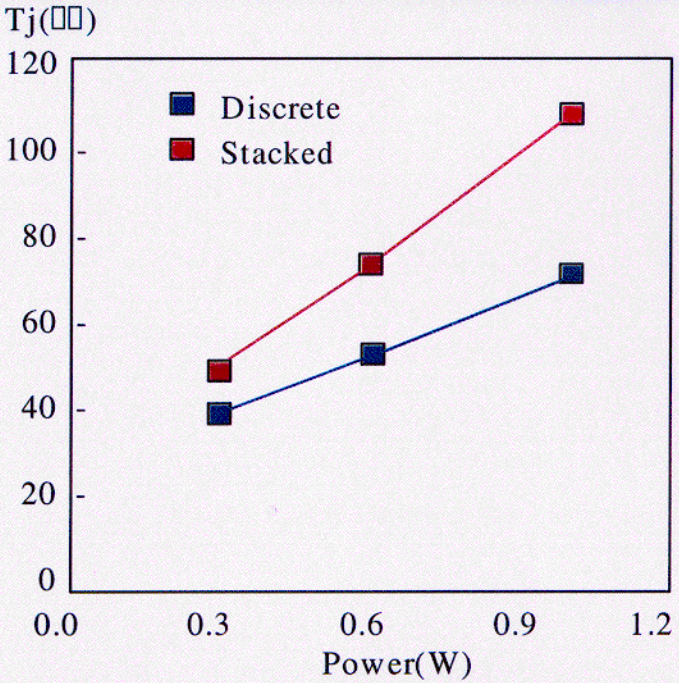
Procondition

★Bake(125 C)
★Socks(85RH/85 C)
★T/C(-65~155 C)
★I.R Reflow(235 C)

★Bottom side



Thermal resistance Evaluation



<@tRC= 110ns>

device / item	0 lfpm		200 lfpm	
	Stacked DRAM	Discrete DRAM	Stacked DRAM	Discrete DRAM
Tj	103.5 °C @ 70 ℃	89.41 °C @ 70 ℃	93.7 °C/W @ 70 ℃	83.15 °C @ 70 ℃
□ ja	87.8 ℃/W	53.91 ℃/W	65.2 ℃/W	36.54 ℃/W
□ jc	below 10.0 ℃/W	8.0 ℃/W	6.0 ℃/W	5.0 ℃/W

Tj(Junction Temperature), □ ja(Junction Ambient), □ jc(Junction to Case)

Conclusion

- ***Without chip design developes the 128M DRAM by using the conventional plastic packaging technology***
- ***Have been verified Reliability, Electrical Performance and I.R reflow soldering.***
- ***Cost effective and mass productiable process***
- ***Providing one of the easiest high density memory solution.***
- ***Future plan***
  - ***Improve thermal performance***